REMARKS

This amendment is in response to the Official Action dated January 29, 2007. Claims 1, 4-19, and 20-23 are currently pending in connection with the present application. Claims 1, 9, 12, 14, and 20 are independent claims. In this amendment, claims 2, 3, and 19 have been canceled without prejudice or disclaimer to further prosecution of their underlying subject matter, and claims 1, 4, and 15 have been amended. Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

No new matter has been added by this Amendment. Claim 1 has been amended to include the subject matter of former claims 2 and 3. Claim 4 is been amended to conform to the amendments of claim 1. Claim 15 has been amended to overcome the examiner's objection.

Claim Objections

Applicant submits that the amendment to claim 15 overcome the examiner's objections.

35 U.S.C. § 102 Rejections

Claims 1, 2, 3, 5, and 10 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Hashizume (U.S. Patent No. 6,539,511).

Claims 2 and 3 have been cancelled, and the associated subject matter incorporated into independent claim 1.

Hashizume discloses a semiconductor integrated circuit device supporting a boundary scan test. Figure 1B illustrates the Hashizume device, including a DC test circuit 3 that sets and resets a series of flip-flops during testmode operation based on the input provided by the TESTC input line (column 6, lines 46-51; column 8, lines 1-4, lines 32-34). During a testmode operation, DC test circuit 3 sets the values of flip-flop boundary scan registers BSR0-BSR3, and boundary scan registers/logic circuits BLU and BLD (column 6, lines 56-61). This operation changes the output of

the flip-flop boundary scan registers for the next clock cycle. However, **since these registers are flip-flops, the scan registers will continue to output their prior results until the next clock cycle.** Therefore, it is still possible to read the flip-flop registers until one cycle after they are provided with the initial testmode data. Therefore, Hashizume does not prohibit the reading of normal mode data **while** providing testmode data.

With respect to claim 1, Applicant submits the Hashizume fails to teach or suggest "*an output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode from said semiconductor integrated circuit.*" As discussed above, while Hashizume overwrites the scan registers one cycle after issuing a test mode signal, Hashizume does not prohibit the reading of normal mode data until one cycle after issuing the test signal. Therefore, Hashizume does not output data during a test mode **while** prohibiting the outputting of data from normal operation. Instead, Hashizume issues a test mode output and, thereafter, one cycle later overwrites the output registers thereby removing the normal mode data. Hashizume fails to disclose the concurrency of the results evident in Applicant's independent claim 1.

Therefore, Hashizume fails to disclose, teach, or suggest various features of independent claim 1. Furthermore, claims 5 and 10 overcome Hashizume because they derive from independent claims 1.

Accordingly, Applicant respectfully requests that the rejection of independent claim 1 and dependent claims 5 and 10 under 35 U.S.C. § 102(e) be withdrawn.

35 U.S.C. §103 Rejections

Claims 4 and 12 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere et al.(U.S. Patent No. 3,961,254); Claims 6, 7, and 11 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Tamamura et al.(U.S. Patent No. 6,118,316); Claim 8 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Bae et al. (KR 200101164); Claims 9 and 19 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere; Claim 13 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of DeLisle et al.(U.S. Patent No. 5,283,889); Claims 14 and 15 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere; Claims 16 and 17 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere et al., in further view of Tamamura; Claim 18 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere, in further view of Bae et al.; Claims 20, 22, and 23 have been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Tamamura et al.; Claim 21 has been rejected under 35 U.S.C. § 103 as being unpatentable over Hashizume in view of Cavaliere, in further view of DeLisle et al.(U.S. Patent No. 5,283,889).

As previously described Hashizume does not disclose, teach, or suggest at least the features of "*an output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode from said semiconductor integrated circuit*" recited in independent claim 1. Independent claims 9, 12, 14, and 20 also include similar subject matter to claim 1, not found in Hashizume. Furthermore, dependent claims 4-8, 10, 11, 13, 15-18 and 20-23 derive from the independent claims and therefore include the features of the independent claims not found in Hashizume.

Cavaliere discloses an LSI semiconductor device, including circuitry for testing embedded memory arrays. Cavaliere does not disclose a technique for prohibiting normal mode output, while supplying testmode data.

Tamamura discloses a semiconductor integrated circuit for generating a stabilized oscillation signal based on an input signal. Even a cursory review of Tamamura shows that Tamamura fails to disclose a technique for prohibiting normal mode output while supplying testmode data.

DeLisle discloses an integrated circuit having a reset signal, but not a testing mode. DeLisle fails to disclose a technique for prohibiting normal mode output while supplying testmode data.

Bae discloses a clock generating apparatus capable of generating test pulses synchronized with another clock signal. However, Bae fails to disclose a technique for prohibiting normal mode output, while supplying testmode data.

Even assuming, arguendo, that Hashizume, Cavaliere, Tamamura, and Bae were combinable (which Applicant does not admit), Applicant submits that none of the cited references of Cavaliere, Tamamura, and Bae, either alone or in any proper combination, cure the deficiencies of Hashizume with respect to at least the previously identified features of claim 1, 9, 12, 14, and 20. Furthermore, at least for the reason disclosed above, claims 4, 6-8, 11, 13, 15-18, and 21-23 also overcome the combination of Hashizume, Cavaliere, Tamamura, and Bae because they derive from the independent claims.

Therefore, Applicant respectfully requests that the rejection of independent claims 9, 12, 14, and 20 and dependent claims 4, 6-8, 11, 13, 15-18, and 21-23 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2810 from which the undersigned is authorized to draw.

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Respectfully submitted,

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